FLASH-ROM MODULE 32MByte (16M x 16-Bit)
Part No. HMFN16M16M8G

GENERAL DESCRIPTION

The HMFN16M16M8G is a high-speed NAND flash read only memory (FROM) module containing 16,777,216 words organized in a x16bit configuration. The module consists of eight 4M x 8 FROM mounted on a 72-pin, double-sided, FR4-printed circuit board.
Data in the page can be read out at 50ns-cycle time per byte.
HMFN16M16M8G extended reliability of 1,000,000 program/erase cycles by providing either ECC (Error Correction Code) or real time mapping out algorithm.
HMF16M16M8G is has address multiplexed into 16 I/O's . Command, address and data are all written through I/O's by bringing /WE to low while /CE is low. Data is latched on th e rising edge of /WE. Command Latch Enable (CLE) and address Latch Enable (ALE) are used to multiplex comma nd and address respectively, via the I/O pins.

FEATURES

- High-density 32MByte design
- Single + 5V ± 0.5V power supply
- Command/Address/Data Multiplexed I/O port
- Organization
  - Memory Cell Array: (4M+128K)bit x 8bit
  - Data Register : (512+16)bit x 8bit
- Automatic Program and Erase
  - Page Program: (512+16)Byte
  - Block Erase: (8K+256)Byte
  - Status Register
- Fast Write Cycle Time
  - Program time : 250us(typ.)
  - Block Erase time : 2ms(typ.)
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 1,000,000 write/erase cycle

OPTIONS MARKING

- Packages

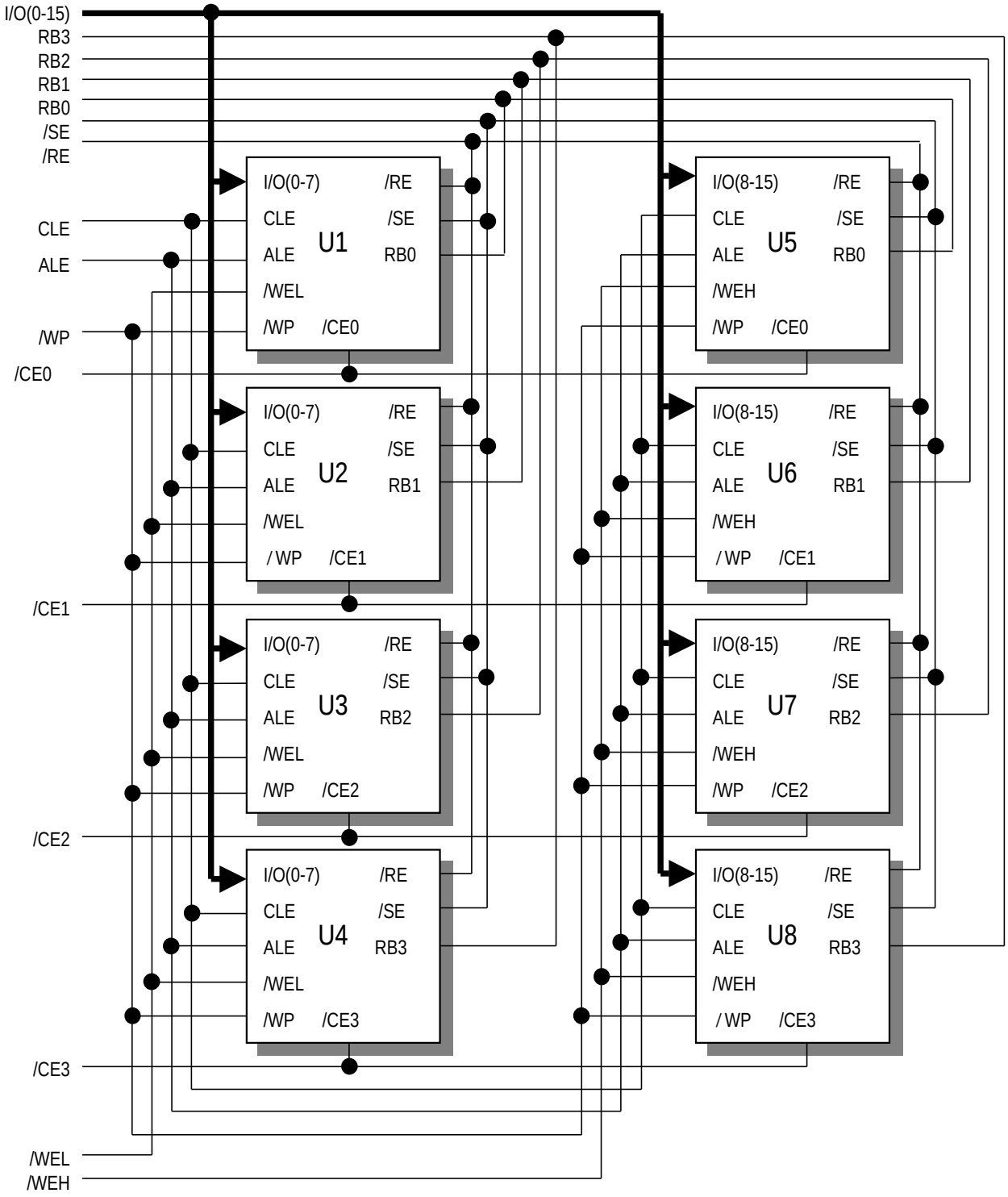
72-pin SIMM	M

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	RB3	49	/CE3
2	I / O0	26	NC	50	/CE3
3	I / O1	27	NC	51	NC
4	I / O2	28	NC	52	NC
5	I / O3	29	NC	53	/WEL
6	I / O4	30	Vcc	54	NC
7	I / O5	31	NC	55	ALE
8	I / O6	32	Vss	56	NC
9	I / O7	33	NC	57	NC
10	Vcc	34	NC	58	NC
11	/CE0	35	/RE	59	Vcc
12	/CE0	36	NC	60	NC
13	NC	37	NC	61	NC
14	/CE1	38	NC	62	NC
15	NC	39	Vss	63	I / O8
16	NC	40	/SE	64	I / O9
17	/WEH	41	NC	65	I / O10
18	NC	42	RB0	66	I / O11
19	CLE	43	RB1	67	I / O12
20	NC	44	NC	68	I / O13
21	NC	45	NC	69	I / O14
22	/WP	46	Vcc	70	I / O15
23	NC	47	NC	71	NC
24	RB2	48	/CE2	72	Vss

72-PIN SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Voltage on any pin relative to Vss	V_{IN}	-0.6 to +7.0	V
Temperature Under Bias	T_{BIAS}	-10 to +125	^{O}C
Storage Temperature	T_{STG}	-65 to +150	^{O}C
Short Circuit Output Current	I_{OS}	5	mA

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70^{O}C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	4.5V	5.0V	5.5V
Supply Voltage	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

PARAMETER		SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Operation Current	Sequential Read	I_{CC1}	tcycle=50ns	/CE=V_{IL},I_{OUT}=0mA	-	15	30	mA
	Command, Address Input	I_{CC3}	tcycle=50ns		-	15	30	mA
	Data Input	I_{CC4}	-		-	15	30	mA
	Program	I_{CC6}	-		-	15	30	mA
	Erase	I_{CC7}	-		-	25	40	mA
Stand-by Current (TTL)		I_{SB1}	/CE=V_{IH},/WP=/SE=0V/Vcc		-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	/CE=Vcc-0.2,/WP=/SE=0V/Vcc		-	10	100	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to 5.5V		-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}= 0 to 5.5V		-	-	±10	uA
Input High Voltage, All inputs		V_{IH}	-		2.0	-	Vcc+0.5	V
Input Low Voltage, All inputs		V_{IL}	-		-0.3	-	0.8	V
Output High Voltage Level		V_{OH}	I_{OH} = -400Ua		2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} = 2.1Ma		-	-	0.4	V
Output Low Current(R/$\overline{B}$)		$I_{OL}(\overline{R/B})$	V_{OL} = 0.4V		8	10	-	mA

AC TEST CONDITON (T_A=0 to +70^{O}C, Vcc =5V±10%, unless otherwise noted.)

PARAMETER	VALUE
Input Pulse Levels	0.4V to 2.6V
Input Rise and Fall Times	5ns
Input and Output Timinig Levels	0.8V and 2.0V
Output Load	1 TTL Gate and CL=100pF

CAPACITANCE (TA=25^{O}C, Vcc=5V, f=1.0M$_{HZ}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	/CE	/WE	/RE	/SE	/WP	MODE	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input(3clock)
H	L	L	↑	H	X	H	Write Mode	Command Input
L	H	L	↑	H	X	H		Address Input(3clock)
L	L	L	↑	H	L/H(3)	H	Data Input	
L	L	L	H	↓	L/H(3)	X	Sequential Read &Data Output	
L	L	L	H	H	L/H(3)	X	During Read(Busy)	
X	X	X	X	X	L/H(3)	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(2)	0V/Vcc(2)	Stand-by	

Note : 1. X can be V_{IL} or V_{IH}

2. /WP should be biased to CMOS high or CMOS low for standby

3. When /SE is high, spare area is deselected.

PROGRAM/ ERASE CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Program Time	t_{PROG}	-	0.25	1.5	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	10	Cycles
Block Erase Time	t_{BERS}	-	2	10	ms

AC TIMING CHARACTERISTICS FOR COMMAND / ADDRESS / DATA INPUT

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
/CE Setup Time	t_{CS}	0	-	ns
/CE Hold Time	t_{CH}	10	-	ns
/WE Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	50	-	ns
/WE High Hold Time	t_{WH}	15	-	ns

AC CHARACTERISTICS FOR OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT
Data Transfer from Cell to Register	t_R	-	10	us
ALE to /RE Delay (Read ID)	t_{AR1}	150	-	ns
ALE to /RE Delay (Read cycle)	t_{AR2}	50	-	ns
/CE to /RE Delay (ID Read)	t_{CR}	100	-	ns
Ready to /RE Low	t_{RR}	20	-	ns
/RE Pulse Width	t_{RP}	30	-	ns
/WE High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
/RE Access Time	t_{REA}	-	35	ns
/RE High to Output Hi-Z	t_{RHZ}	15	30	ns
/CE Hith to Output Hi-Z	t_{CHZ}	-	20	ns
/RE High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to /RE Low	t_{IR}	0	-	ns
Last /RE High to Busy (at sequential read)	t_{RB}	-	100	ns
/CE High to Ready (in case of interception by /CE at read) (1)	t_{CRY}	-	$50+tr(\overline{R/B})$ (2)	ns
/CE High Hold Time (at the last serial read)	t_{CEH}	100	-	ns
/RE Low to status Output	t_{RSTO}	-	35	ns
/CE Low to status Output	t_{CSTO}	-	45	ns
/RE High to /WE Low	t_{RHW}	0	-	ns
/WE High to /RE Low	t_{WHR}	60	-	ns
Erase Suspend Input to Ready	t_{SR}	-	500	us

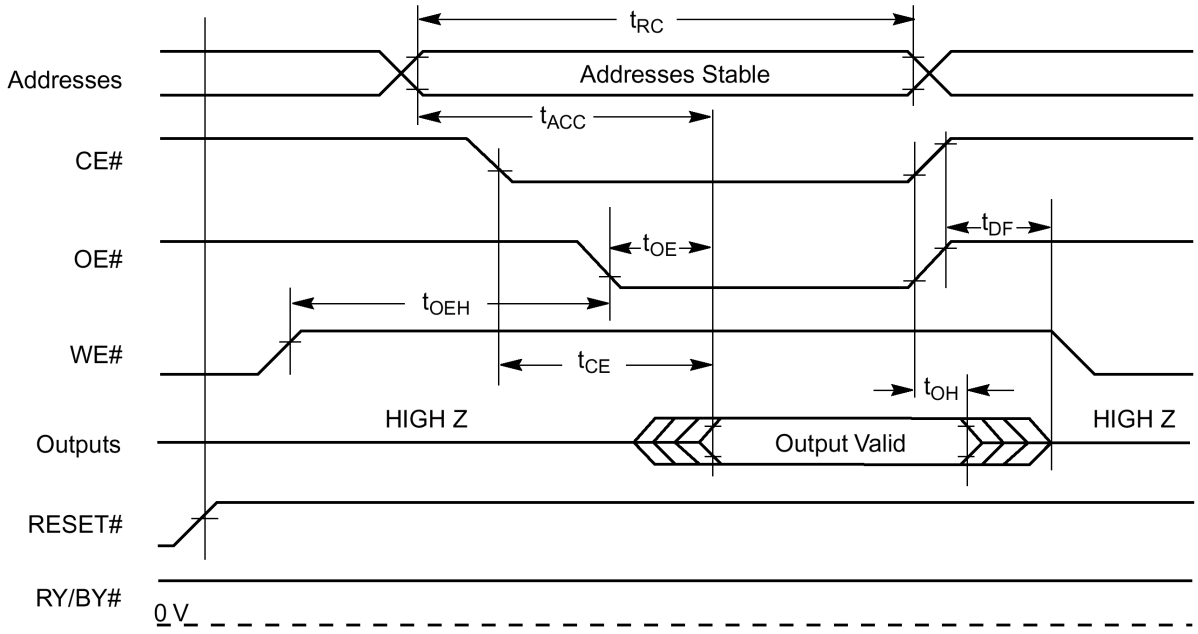
/RE access time (Read ID)	t_{READID}	-	35	ns
Device Resetting Time	t_{RST}	-	5/10/500/5	us

Note: 1. If /CE goes high within 30ns after the rising edge of the last /RE, R//B Will not return to V_{OL}

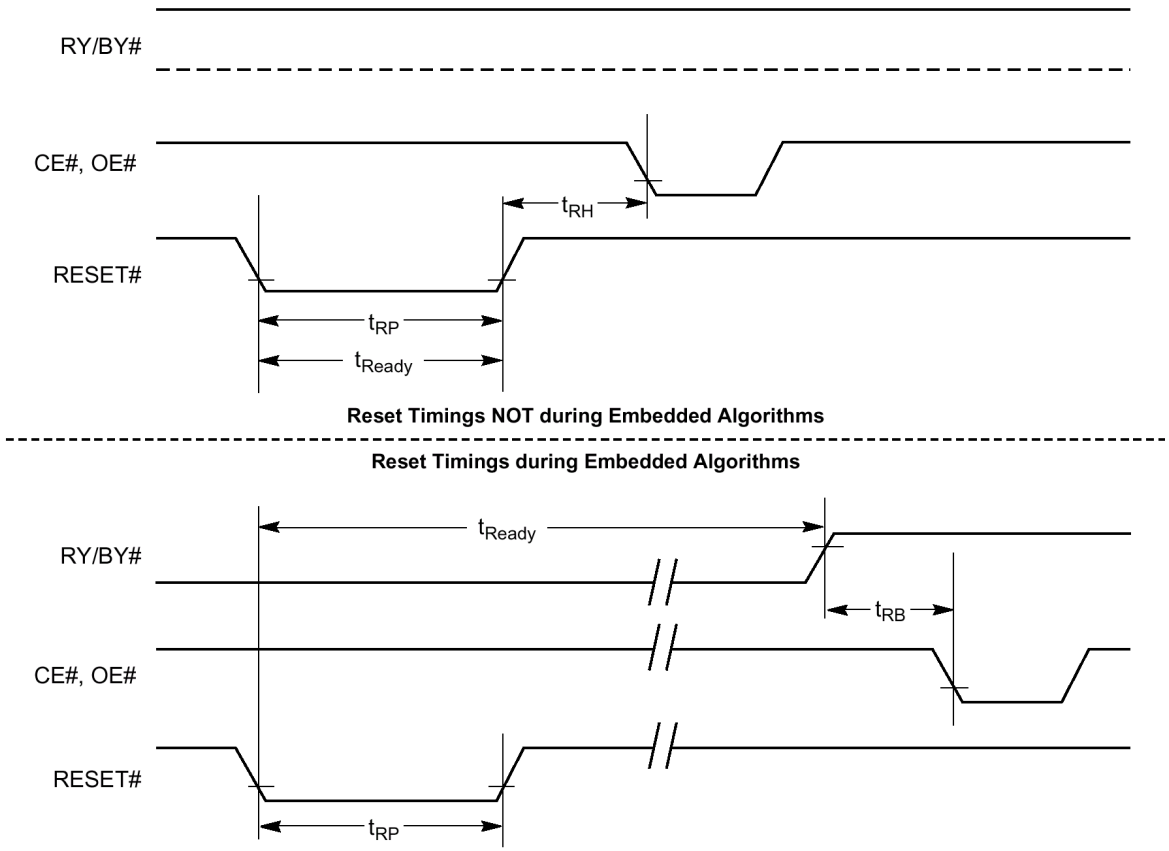
2. The time to Ready depends on the value of the pull-up resistor tied R//B pin

3. To break the sequential read cycle, /CE must be held high for longer than t_{CEH}.

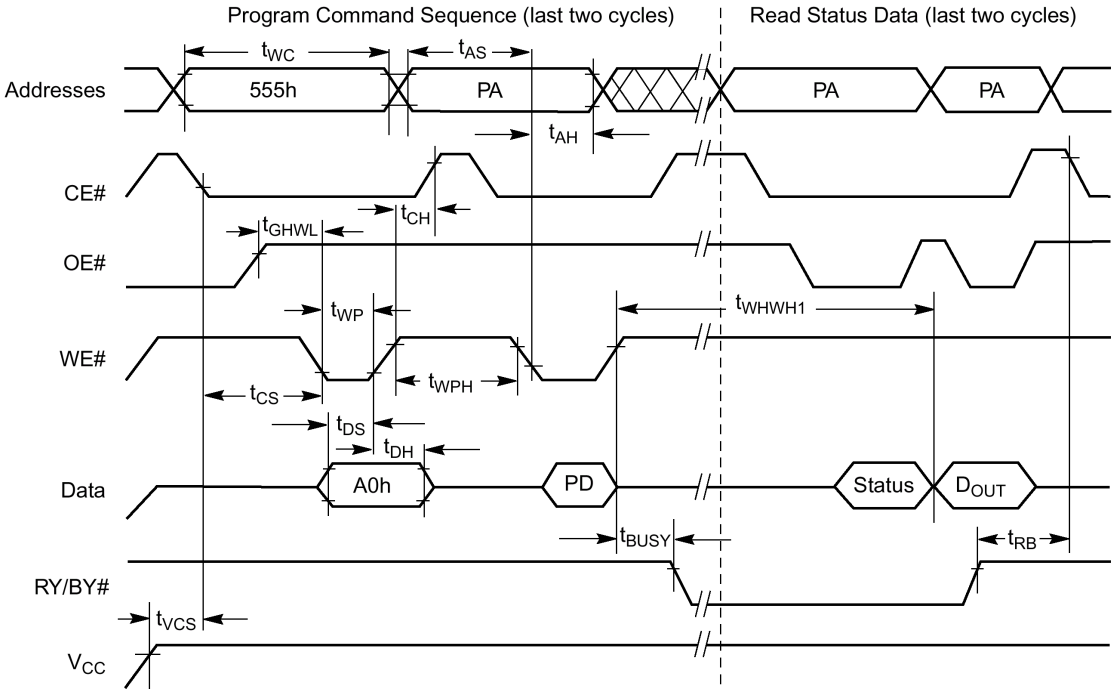
u READ OPERATIONS TIMING



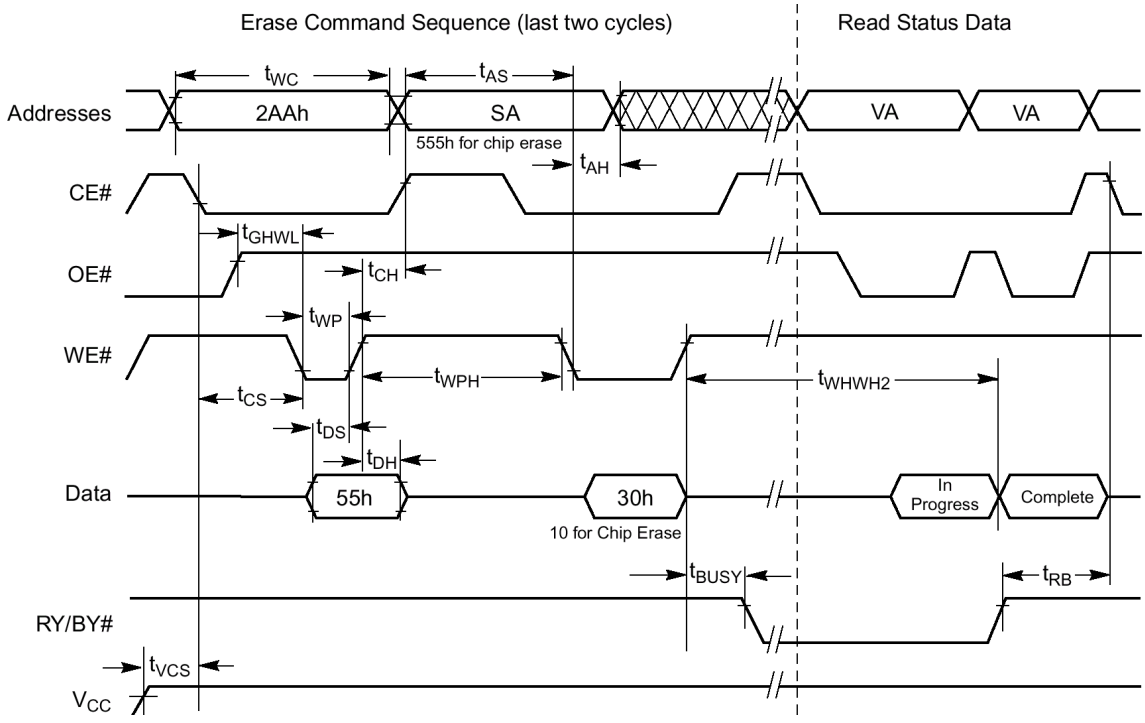
u RESET TIMING



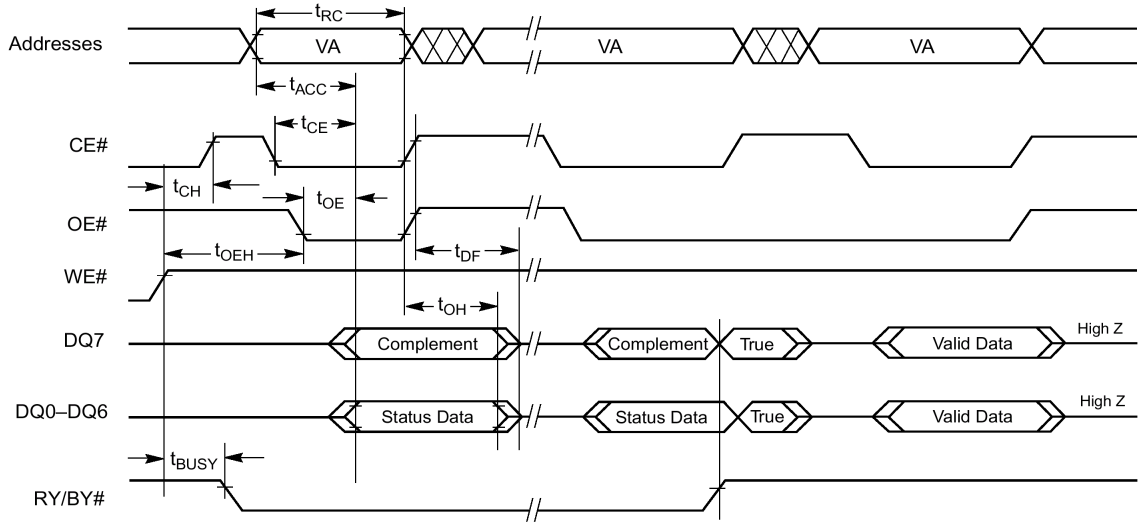
u PROGRAM OPERATIONS TIMING



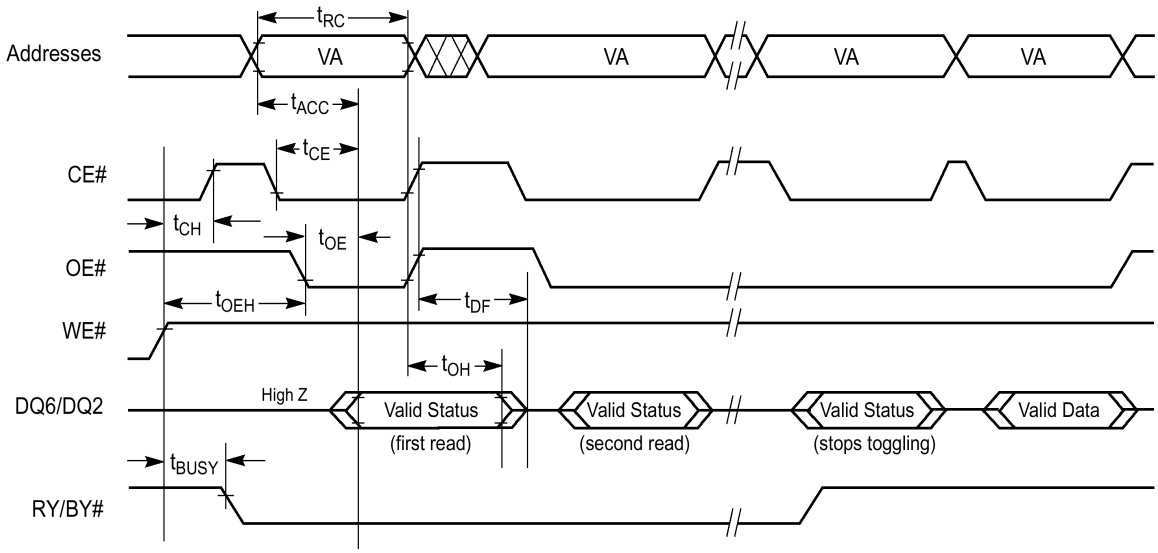
u CHIP/SECTOR ERASE OPERATION TIMINGS



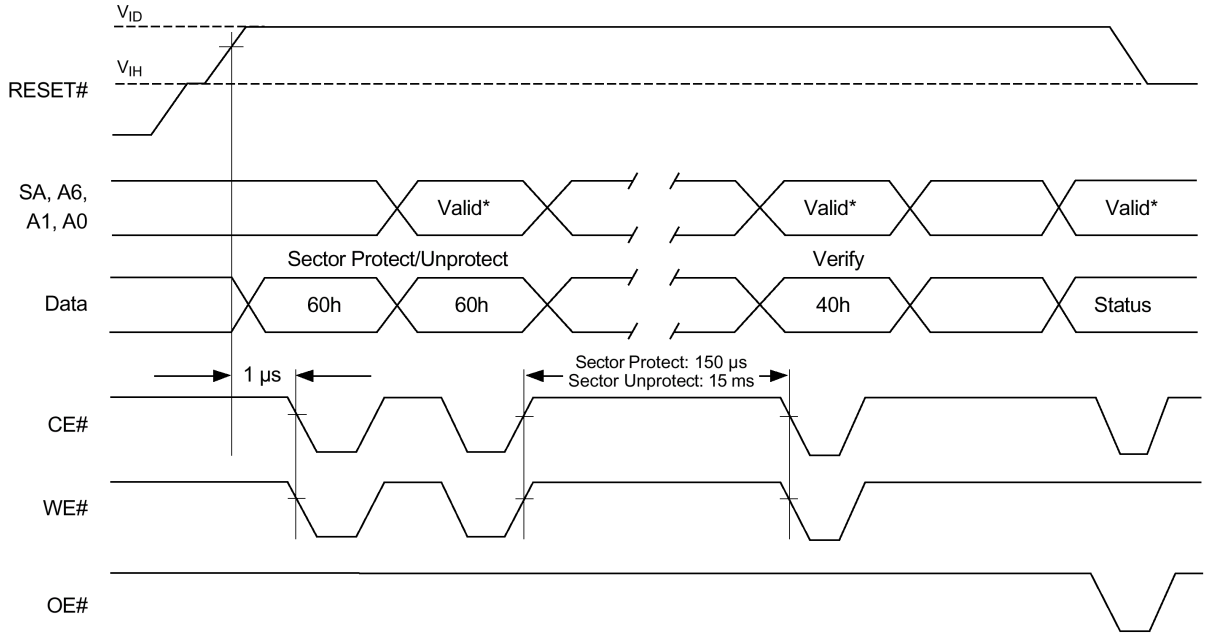
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



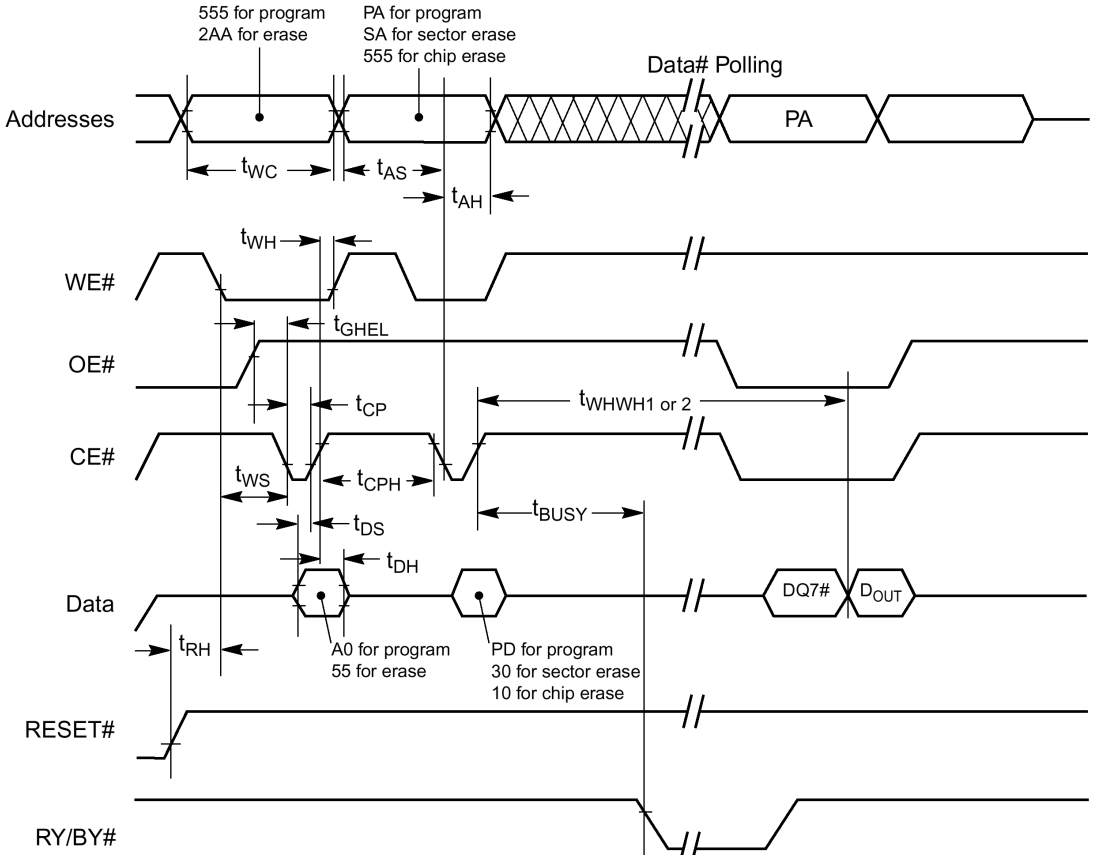
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



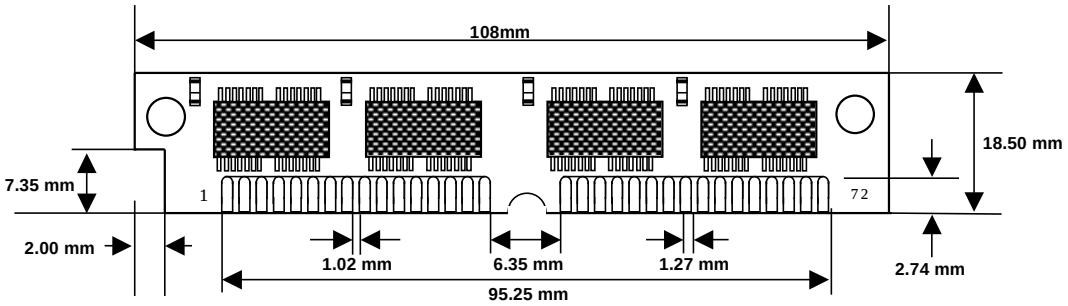
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

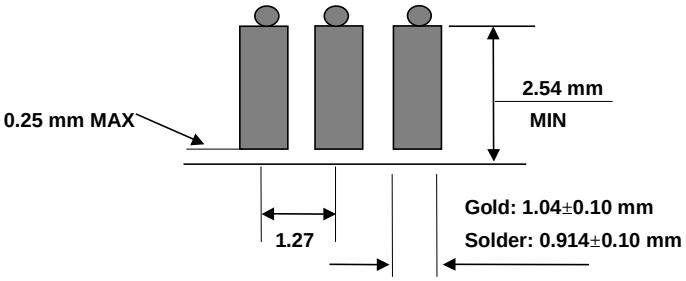


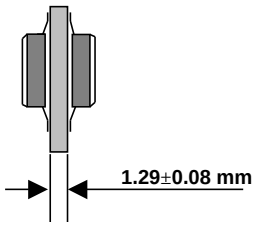
u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS







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(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	Function
HMFN16M16M8G	32MByte	16MX 16bit	72 Pin-SIMM	8EA	5V	NAND,Perfect Sector